Introductory Exercise 5: Basics Of Circuit Board Modeling

In the first part of the exercise, you will model the single component board shown in Figure 2-27:

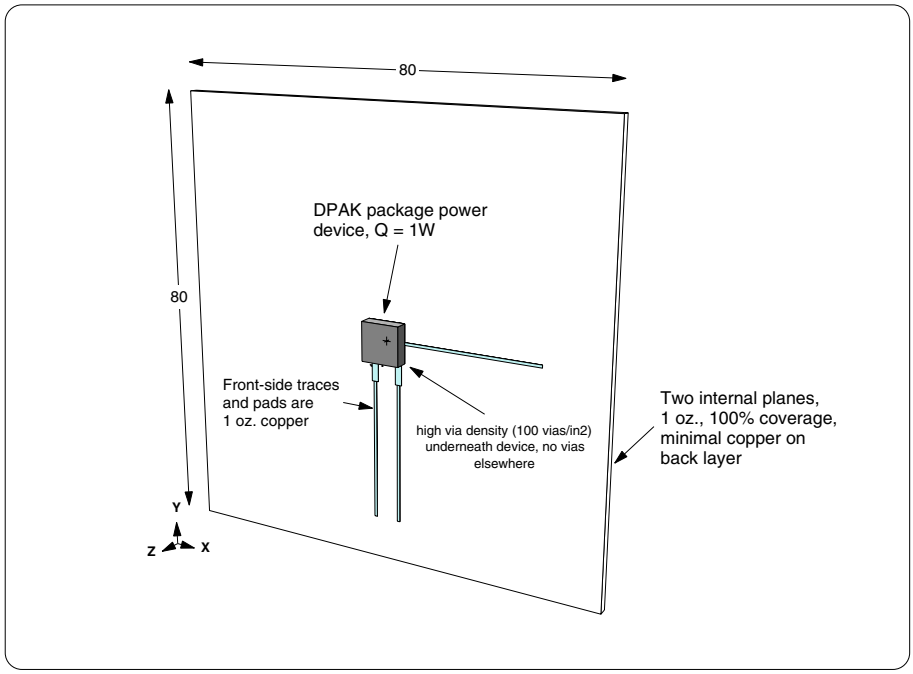


Figure 2-27: Circuit board for exercise 5

Note that this board includes two full internal planes (ground and power). The pad underneath the device is connected to the first internal plane with thermal vias. It is assumed that there is a limited number of traces and pads on the back side of the board.

After modeling this simple board, you will add two dual SOIC devices. Then you will add a 64 lead QFP with heat slug (see Figure 2-38 on page 2-87).

Prerequisites

Some users are only interested in modeling circuit boards. There is no interest in modeling heat sinks or boxes. For these users, it is tempting to start with this exercise, rather than beginning with *Introductory Exercise #1: A Simple Finned Heat Sink.* However, this is strongly discouraged. The earlier exercises introduce important concepts and techniques. So if you plan to be a regular user of Sauna, you need to work all of the introductory exercises.

Planar vs. detailed stackup model

Sauna provides two different methods for modeling circuit boards: planar and detailed stackup. The planar method is a simplified approach, which has been in use for over a decade. In this type of model, there is no ΔT between the faces of the board. For a multilayer board, you can think of all the layers as being “smashed” together. Also, with the planar approach, you do not model individual traces and pads. Instead, the copper coverage is modified. Other software packages use a similar approach and define a parameter known as the "copper volume percentage".

As the name implies, the detailed stackup method is more precise. With this method you will create individual traces and pads, such as the traces shown on the front layer in Figure 2-27. You will also modify the via density, so you will be able to add the vias underneath the MOSFET device. While this method is more precise, note that you will usually not model every trace and via on the board. Instead, you will model the traces and pads in the key areas around heat generating components, while using less detail in other areas (more on this later).

So which approach is best? If you are new to Sauna, you might think that the detailed stackup method is clearly superior. But, as experienced Sauna users know, planar models are valuable in many situations. So you will use both methods to model the board shown above. As you will see, for the simple board in Figure 2-27, you will end up with similar results.

Creating a planar model

To create the planar board model, start with these commands:

<F12 Root Menu> → Model → Assembly → Circuit Brd → "planar" → Rectangle → Vertical XY → "80,80" → .062"/1.6mm → (0,0,0) → FR4

You will reach the Copp Layers menu:

```
  COPP LAYERS
> 1 Zer/Lam Only
  2 One
  3 Two
  4 Three
  5 Four
  6 Six
  7 Eight
  8 Enter Layers
```

The first selection, "Zer/Lam Only", stands for "zero copper layers/laminate only". *This selection is used with the detailed stackup method.*

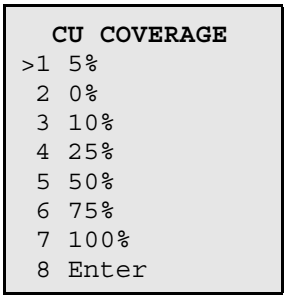
The remaining selections are for planar models. You will be specifying the total number of copper layers in the board. Since the board shown in Fig 2-27 has four copper layers (two internal planes, two outer layers), continue with:

Four

Next, the Cu Weight menu will be displayed. With this menu, you will choose the thickness of the copper plating. By industry convention, thickness is expressed with ounces: copper plating weight per square foot of surface area. The thickness of a one ounce copper layer is 0.036 mm (0.0014"). Continue with:

One oz.

The Cu Coverage menu will be displayed:



With the planar method, you will not model individual traces and pads on the board. Instead, you will define a "copper coverage", which is the average copper percentage for all board layers combined. The current board has 100% copper for the internal planes and close to 0% copper for the outer planes. So the average across all four layers is roughly 50%. Complete creation of the board with:

50%

The board assembly will be created and drawn on the screen. Board assemblies are drawn with a green color, so it's easy to distinguish between a board assembly and a plate assembly. The default node spacing for boards is 5 mm, since board components tend to be smaller than heat sink components.

Use the Info command to generate a report:

<F7 Info> → Trap → Board → ***trap the board***

As for plates, a complete report will be displayed on the screen. Since the report describes a circuit board, information is provided on copper weight, number of layers, etc.

Clear the report from the screen before continuing.

The importance of copper

Now you will do some experiments to see how important a role copper plays in allowing heat to spread throughout the circuit board. As shown in Figure 2-28 on the next page, zoom in with:

<F3 Zoom In> → ***zoom in as shown in Figure 2-28***

Next, make resistor values visible:

<F6 Setup> → Display → Resistor → Numeric Rth → On

The current resistor value of 35.77°C/W will be displayed. Note that "Numeric Rth" stands for "numerical $\mathbf{R}_{\text{thermal}}$".

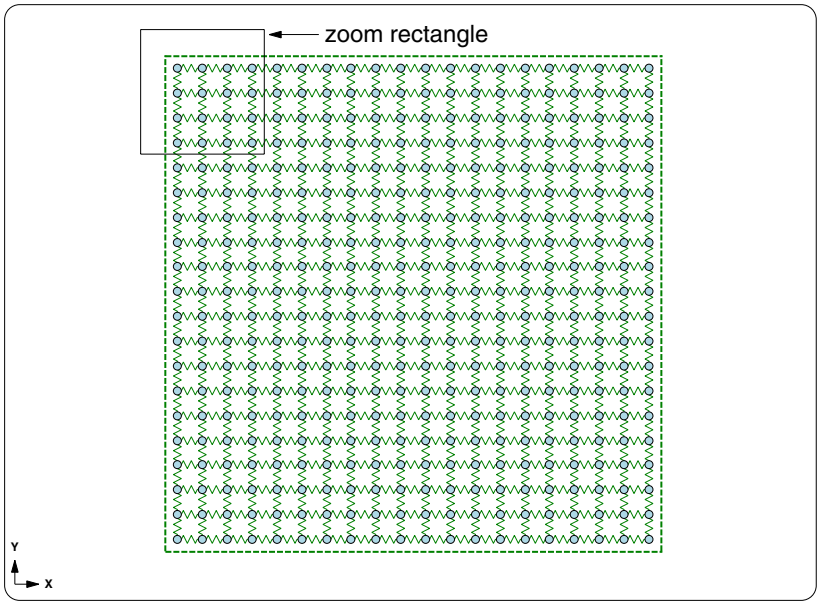


Figure 2-28: Zooming in on circuit board

Now let's see what happens when the copper coverage is decreased by a factor of two (from 50% to 25%):

<F12 Root Menu> → Edit → Plate/Board → Board Props → Cu Coverage → 25% → Entire Brd → Group → All In Wind → USE

When the copper coverage is reduced, the resistance values increase. The resistance value is now 70.29°C / W, nearly double the previous value. This tells us that the **board's thermal resistance is almost exclusively dependent on the copper**. The FR4 laminate material is a poor heat conductor and has little impact on the thermal resistance.

The copper coverage can be modified for the entire board, or for just some of the nodes. Modify copper coverage to 100% for the nine nodes in the top-left corner:

<F12 Root Menu> → Edit → Plate/Board → Board Props → Cu Coverage → 100% → Node Group → Select Regn → *grouping rectangle includes 9 top-left nodes* → USE

With this change the resistance value decreases to 18.05°C / W.

Return to 50% copper coverage for the entire board:

<F12 Root Menu> → Edit → Plate/Board → Board Props → Cu Coverage → 50% → Entire Brd → Group → All In Wind → USE

Once again, you will see R = 35.77°C / W. Restore the display setup and resize the window:

<F6 Setup> → Display → Resistor → Use Default

click 

Completing the planar model

With a just a few more steps, you can complete the planar model. First, add the heat source:

<F12 Root Menu> → Model → Heat Input → Basic Source → "1" → "S1" → DPAK → Typical → Solder 0.1mm → One → *trap board* → Coords/Trap → "40,40"

Notice that you used “typical” for the junction-to-case resistance. For the DPAK package, the typical value is R_{jc} = 1.8°C / W.

As you have done in previous exercises, align the mesh to the heat source:

<F12 Root Menu> → Edit → Plate/Board → Remesh/Align → Align Mesh → Heat Source → 4 Node Conn → *trap heat source* → All In Wind → USE

The board will be realigned. Next, add float resistors on both sides of the board:

<F12 Root Menu> → Model → Amb + Float → Isoltd->Fix → "Room Amb" → Natural → Both Sides → All In Wind → USE

click 

Now you are ready to calculate temperatures:

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

You should obtain T_{junct} = 45.91°C. Now that you have quickly obtained a temperature, you can delete the planar model:

<F12 Root Menu> → Delete → Everything → *click Yes button*

The detailed stackup method (checklist)

Now you are ready to model the same board with the detailed stackup method. Here's a description of the method:

1. Create a "zero copper layer" board assembly. This is a laminate (dielectric) layer. Normally, you should use the default label of “Lamin>1”.

2. For the front side components, use Sauna's library to create traces and pads . (For non-standard components, use the methods described in *Intermediate Exercise 3: More On Circuit Board Modeling*.)

3. Create enhanced heat sources on top of the pads created in step #2.

4. If necessary, edit the resistance between the enhanced heat source junction and the lead pads.

5. If necessary, create additional traces and pads.

6. Align the board, traces and pads to the most important heat source on the board. To align to more than one heat source, use the method described in *Intermediate Exercise 3: More On Circuit Board Modeling.*

7. Although not an absolute requirement, it is recommended that you add float resistors and perform a preliminary calculation.

8. If you performed a preliminary calculation, delete the float resistors and ambient nodes.
9. Subdivide the laminate assembly to create internal layers.
10. Change the via density in the appropriate areas.
11. If necessary, repeat steps #2 - #5 for the back layer.
12. Add float resistors and ambient nodes.
13. Calculate temperatures.

You will be following these steps as you work through the exercise. The above checklist is quite useful when modeling board stackups. You may wish to mark this page of the manual so you can find it later.

Step #1: create zero copper layer board assembly

The first step is the creation of a laminate-only board assembly. In the terminology of Sauna, this is a "zero copper layer board". Create the board:

<F12 Root Menu> → Model → Assembly → Circuit Brd → *hit <Enter> to skip*
→ Rectangle → Vertical XY → "80,80" → .062"/1.57mm → (0,0,0) → FR4
→ Zer/Lam Only → .025"/0.64mm → One oz. → None

An 80 mm x 80 mm board assembly will be created. Since you did not directly specify a label, the board label will be "Lamin>1", which is the default for zero layer boards. This is the recommended approach. Notice that you defined via properties (0.025" diameter, 1 oz plating), even though the density is currently set to zero. Later, when a via density is assigned, these via properties will be used.

As a comment, you could have used the planar board as your starting point. But if you start with a planar board, there's a number of board properties to modify. So it's usually simpler, and less error-prone, to start over.

Step #2: use Sauna's library to create traces and pads

Now you are ready to create the pads for the DPAK enhanced source. Sauna has a library of over 200 different package styles, including several variation of DPAK's. Begin with:

<F12 Root Menu> → Model → Assembly → Trace/Pad → Board Side → *trap board* → Component
→ One oz. → Pad Library

You will reach the Pad Library menu:

```
 PAD LIBRARY
1 DPAK's
2 TDSON/TOLL
3 Single/Dual
4 Quad
5 Diodes
6 LED's
7 Resistor
```

With enhanced sources, you do not have to define individual rectangles for the pads. You just need to pick the component type and the placement point. Complete creating the pads:

DPAK's → DPAK → 2 → Same As Body → Pad Only → 0 Degrees → Coords/Trap → "40,40"

The pads will be created, as shown in Figure 2-29. Note that there is a reference point, which will make it easy to place the enhanced source on these pads.

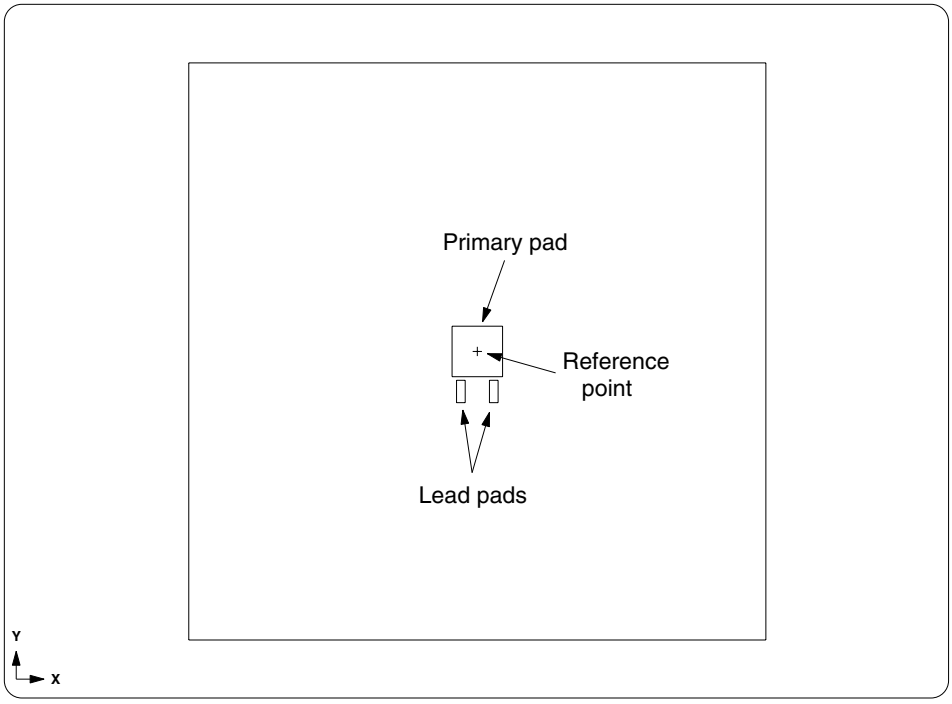


Figure 2-29: DPAK pads

Step #3: create enhanced heat source

With the pads created, you are ready to add an enhanced heat source. An enhanced heat source is a more complete model of a power component. With a basic heat source, the only heat flow path is through the bottom of the component. The enhanced source, on the other hand, allows for multiple heat flow paths, including lead connections and heat sinks placed on top of the component.

Begin creating the enhanced source:

<F12 Root Menu> → Model → Heat Input → Enhanced Src → DPAK's → "1" → "S1" → DPAK → 2 → Typical

You will reach the R_Lead_Pad menu:

```
  R LEAD PAD
>1 Typ-1500 C/W
 2 Enter Resis
 3 Enter R para
 4 No Lead Conn
```

The R_Lead_Pad menu is used to specify the resistance between the enhanced source junction and the lead pads. The problem with $R_{junct\text{-}to\text{-}lead\text{-}pad}$ is that it is generally not on the datasheet and is rather difficult to obtain. But Thermal Solutions has determined that 1500°C / W is a reasonable typical value to use, primarily based on published data from Infineon and Amkor.

Finish creating the enhanced source:

Typ-1500 C/W → Ref Point → ***trap reference point***

The enhanced heat source will be created. If you look closely at the screen, you will see that there is an additional assembly. This is the body assembly associated with the enhanced heat source. You can see this best in a shaded perspective view:

click  **→** ***click*** 

The screen will be as shown in Figure 2-30.

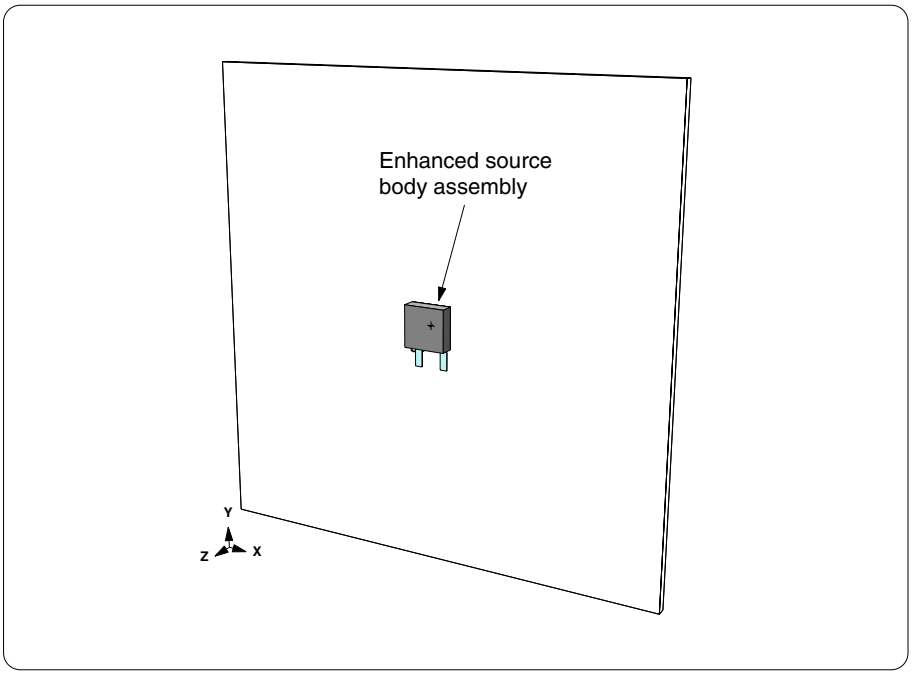


Figure 2-30: enhanced heat source with body assembly

Return to a front view and get an Info report for the heat source:

click Front

<F7 Info> → Trap → Node → Heat Source → ***trap S1 source***

On the second page of the report, a variety of important information is provided. For example, you can see that R_{jc} = 1.80°C / W and $R_{junct\text{-}to\text{-}top}$ = 37.94°C / W. The last section shows that there are two lead pad connections with $R_{junct\text{-}to\text{-}lead\text{-}pad}$ = 1500°C / W.

Clear the report from the screen before continuing.

Step #4: edit resistance between the enhanced source junction and lead pads

In step #4, you would modify the resistance between the enhanced source node (which always represents a junction) and the lead pads. When you created the source, you assumed a $R_{junct\text{-}to\text{-}lead\text{-}pad}$ of 1500°C / W for both leads. Be aware, if the DPAK device is a power MOSFET, the thermal resistance is probably lower for the high current lead (source) than for the gate lead. So if you wanted to modify $R_{lead\text{-}pad}$, it would be done in step #4. However, Thermal Solutions has obtained good accuracy for DPAK's with the default resistance for both leads. So nothing needs to be done for this model.

Step #5: create additional traces and pads

Now you need to add the traces shown in Figure 2-27. These traces are 0.5 mm wide by 25 mm long. When complete, the model will be as shown in Figure 2-31 on the next page. Add a trace to the left lead pad:

<F12 Root Menu> → Model → Assembly → Trace/Pad → Trap Trc/Pad → ***trap any pad***
→ Trace/1 Seg → Trap Trace → ***trap lower edge of left lead pad***
→ Define Delta → Dy → "-25"

The trace will be created. Add a trace to the right lead pad:

Trace/1 Seg → Trap Trace → ***trap lower edge of right lead pad*** **→ Define Delta → Dy → "-25"**

The new traces picked up a width of 1.2 mm from the lead pads. Change the trace width to 0.5 mm (.020”):

Edit Width → 0.50mm/20mil → Entire Trace → Select Regn
→ ***grouping rectangle to include both 25 mm traces*** **→ USE**

Now you need to add the trace to the right of the primary pad (large pad underneath DPAK). It’s a little easier if you begin by turning off the heat source:

<F12 Root Menu> → Visibility → Turn Off → Node/Resis → Node Group → Heat Source
→ Any Source → All In Wind → USE

Zoom in on the primary pad:

<F3 Zoom In> → ***zoom in on primary pad***

Add the trace which is connected to the primary pad:

<F12 Root Menu> → Model → Assembly → Trace/Pad → Trap Trc/Pad → ***trap any trace or pad***
→ Trace/1 Seg → Width/Point → 0.50mm/20mil → Midpoint
→ ***trap upper-right corner of primary pad*** **→** ***trap lower-right corner of primary pad***
→ Define Delta → Dx → "25"

The third trace will be added. Turn on all model elements and return to the Root menu:

click 

<F12 Root Menu>

Zoom out and activate shade mode:

click  **→** ***click*** 

The screen should be as shown in Figure 2-31. Make sure that the body assembly is visible, which indicates that the heat source is turned on.

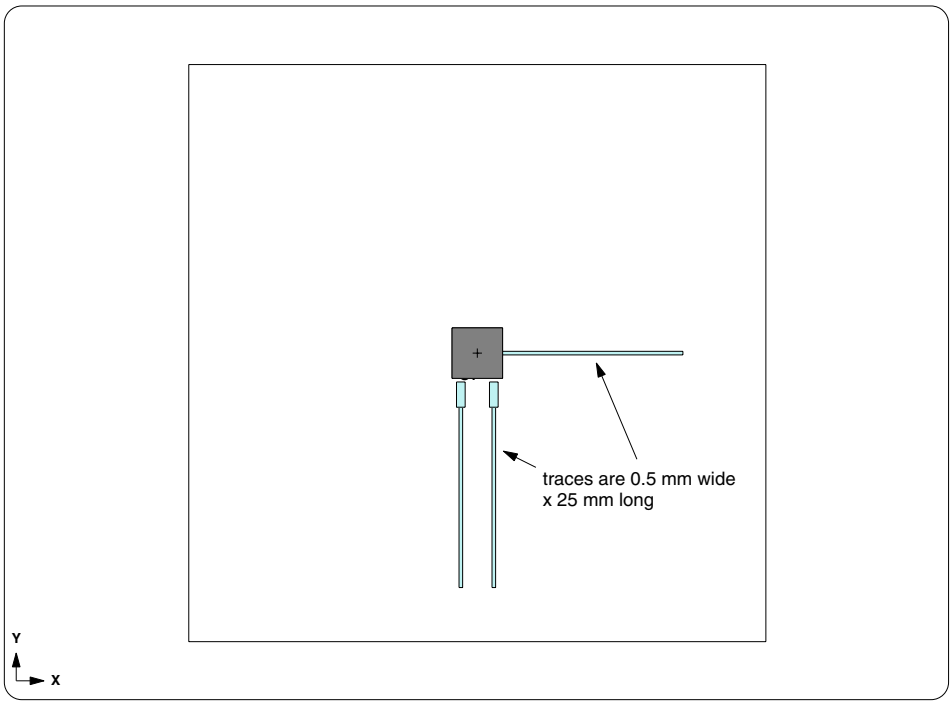


Figure 2-31: Model with three 25 mm traces

Step #6: align to heat source

Align the board and pads to the heat source:

<F12 Root Menu> → Edit → Plate/Board → Remesh/Align → Align Mesh → Heat Source → 4 Node Conn → ***trap heat source*** **→ All In Wind → USE**

The board and pads will be aligned to the heat source.

Step #7: add float resistors and perform preliminary calculation

At this point, the front layer is fully defined. The checklist calls for a preliminary calculation. Although the model is not complete, the preliminary calculation lets you check for errors and make corrections while the model is still simple. Also, even though the internal planes are missing, you will still get some idea of final temperatures. For example, if temperatures are moderate with just a single copper layer, you should be in good shape when the internal planes are added.

Create float resistors:

<F12 Root Menu> → Model → Amb + Float → Isoltd->Fix → "Room Amb" → Natural → Both Sides → All In Wind → USE

click 

Calculate temperatures:

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

You should obtain $T_{S1\text{-}junct}$ = 172.36°C. A junction temperature of 172.36°C is high, but temperatures should be significantly cooler when the internal planes and vias are added.

This model will be used later in the exercise. Save the model as "dpak_single_lyr.smf":

<F12 Root Menu> → File → Save As → *type "dpak_single_lyr" in File name box* → *click Save button*

What-if #1: modifying trace lengths

Normally, after completely a preliminary calculation, you will delete the float resistors and then create the internal layers. However, you will stop following the checklist so you can experiment with changing the length of the traces.

It's useful to view the temperatures contours.

click 

As you look at the contours, you can see the traces are at elevated temperatures, suggesting that they contribute to heat transfer from the component. On the other hand, notice that the end of the traces are rather cool. So perhaps long traces don't really help much. The purpose of this section is investigate these issues.

When you add, modify or delete traces, you will need to delete the float resistors and ambient nodes:

click 

<F12 Root Menu> → Delete → Node → Fixed → All In Wind → USE

As the first part of the what-if investigation, you will delete all three traces, so you can see the size of the temperature increase:

<F12 Root Menu> → Delete → Assembly → Plate → *place 3 traces in group* → USE

The traces will be deleted. If you are confused by "place 3 traces in group", see the top of page 2-56. Note that traces and pads are classified as plate assemblies.

Now add float resistors:

<F12 Root Menu> → Model → Amb + Float → Isoltd->Fix → "Room Amb" → Natural → Both Sides → All In Wind → USE

click 

Calculate temperatures:

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

You should obtain T_{junct} = 188.96°C. This is an increase of 16.6°C, or 11.3% (based on the ΔT). *So the 0.5 mm wide traces definitely help cool the part.*

Next, let's see what happens if the traces are made longer. Begin by using Undo to restore the traces:

<F12 Root Menu> → Edit → Undo → ***click Yes button to undo Amb + Float***

<F12 Root Menu> → Edit → Undo → ***click Yes button to undo delete***

You will increase the length of all three traces by 5 mm. Begin with the right horizontal trace:

<F12 Root Menu> → Edit → Plate/Board → Dimensions → Trace/Pad → Shift Endpt → *trap right edge of horizontal trace* → Define Delta → Dx → "5"

The trace will be extended by 5 mm. Extend the two vertical traces:

Shift Endpt → ***trap lower edge of left vertical trace*** **→ Define Delta → Dy → "-5"**

Shift Endpt → ***trap lower edge of right vertical trace*** **→ Define Delta → Dy → "-5"**

With these changes, all three traces have been extended by 5 mm to a total length of 30 mm. Add float resistors and calculate temperatures:

<F12 Root Menu> → Model → Amb + Float → Isoltd->Fix → "Room Amb" → Natural → Both Sides → All In Wind → USE

click 

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

You should obtain T_{junct} = 172.29°C. Extending the traces by 5 mm only reduced temperatures by 0.07°C, or just 0.05%. So there was almost no impact.

In thermal modeling there is a rule of thumb that states **traces longer than 25 mm (1 inch) have no effect on cooling**. So far, this rule seems valid. But it will be interesting to see what happens when the traces are shortened.

As the last part of this what-if section, you will work on your own to shorten all three traces from 30 mm to 15 mm. Don't forget to delete float resistors before modifying the trace length. After modifying the traces, add float resistors and calculate temperatures at 25°C.

When complete, you should obtain T_{junct} = 173.22°C. When comparing the 15 mm trace length to the original 25 mm trace length, temperatures are only slight hotter (0.86°C or 0.6%). So 15 mm traces are nearly as effective as 25 mm traces.

What does this say about the rule "traces longer than 25 mm (1 inch) have no effect on cooling"? The rule is generally valid, but it's a bit conservative since the 15 mm traces are almost as effective as 25 mm traces.

Also, please be aware that traces will be less important when internal planes are added. For heat slug components on multilayer boards with thermal vias, heat transfer through the traces is fairly limited (more on this later).

Finally, restore the traces to 25 mm length and recalculate temperatures. You should once again obtain T_{junct} = 172.36°C. (Note that you also have the option of simply reloading dpak_single_lyr.smf.)

When complete, the model will be back to the condition at the end of "Step #7: add float resistors and perform preliminary calculation".

Step #8: delete the float resistors and ambient nodes

In this step you delete the float resistors created for the preliminary calculation:

click 

<F12 Root Menu> → Delete → Node → Fixed → All In Wind → USE

Board stackup report and assembly labeling

In a moment you will create the internal copper planes. But before starting, it's very useful to obtain a board stackup report:

<F7 Info> → Assemblies → Brd Stackup → All → Current → Screen

The report gives the key parameters for the board stackup. This includes the copper weight, laminate thickness and via density. At the moment, there is just one laminate layer and it is identified as "Lamin>1", which is the label of the zero layer board. Later in the exercise, when you subdivide the board to create two internal copper planes, the new laminate layers will be labeled "Lamin>2" and "Lamin>3". You should remember the labeling scheme because it provides an easy way to select a board assembly when grouping.

The copper layer is identified as "Copp>1". Unlike the laminate layer, this does not identify any specific assembly. Instead, the traces and pad are automatically labeled according to a "Copp>n>n" format, which will be explained in a moment.

Clear the board stackup report from the screen before continuing.

Now obtain an assembly list report:

List/Supers → Screen

All of the assemblies in the model will be listed on the screen, as shown in Table 2-1 on the next page. The first assembly, "Body>1", is the body assembly associated with the DPAK. Then you see "Copp>1>1" through "Copp>1>6" which are the labels for the traces and pads. Notice that all of the traces and pads on the front layer start with "Copp>1". The first trace or pad on the layer is given the label “Copp>1>1”, the second trace or pad is labeled “Copp>1>2”, etc.

```
                    ASSEMBLY LIST

Assembly           Type Plane  Dimensions
Body>1              Plt   XY   7.00 x 7.00 x 2.30
Copp>1>1            Plt   XY   7.00 x 7.00 x 0.036
Copp>1>2            Plt   XY   1.20 x 3.50 x 0.036
Copp>1>3            Plt   XY   1.20 x 3.50 x 0.036
Copp>1>4            Plt   XY   0.50 x 25.00 x 0.036
Copp>1>5            Plt   XY   0.50 x 25.00 x 0.036
Copp>1>6            Plt   XY   25.00 x 0.50 x 0.036
Lamin>1             Brd   XY   80.00 x 80.00 x 1.57
```

Table 2-1: Assembly list report

When a new copper layer is created, it will be labeled according to the same scheme. So the first internal plane, which is just a large pad, will be labeled "Copp>2>1". The second internal plane will be "Copp>3>1", etc. Once again, remember this labeling method because it can be used to select and isolate copper layers.

Clear the assembly list report. Now you are ready to subdivide the board.

Step #9: subdivide the laminate assembly to create internal layers

Start subdividing with:

<F12 Root Menu> → Edit → Plate/Board → Subdivide → Stackup → Board

You will reach the Board Subdiv menu:

```
  BOARD SUBDIV
>1 Intern Layer
 2 Full Stackup
 3 V4.0 Method
```

As you can see, there are three options for creating a board stackup. "Intern Layer" is the method you will be using. "Full Stackup" is another method, which is based on starting with a planar model. "V4.0 Method" is an older, "quick and dirty", method introduced in Sauna V4.0. This approach is no longer recommended.

Continue with:

Intern Layer

Now you will see the Add Layers menu. For a four layer board, the correct choice is "Two". You have already defined the front layer with the pads for the DPAK. The "Intern Layer" command will provide you with two internal layers (typically a power plane and ground plane). When the internal subdivide is complete, you would create the traces and pads for the back layer. In this way, a four copper layer board is defined.

Complete the subdivide with:

Two → Uniform → One oz. → Typical → All In Wind → USE

The board stackup will be created. Get an Info report for the new stackup:

<F7 Info> → Assemblies → Brd Stackup → All → Current → Screen

The board stackup report shows 3 copper layers and 3 laminate (dielectric) layers. You used the "typical" option, so the laminate thicknesses are 0.396 mm, 0.711 mm and 0.396 mm (.016" / .028" / .016").

Internal planes improve cooling, even when there are no thermal vias. To see this, clear the report, then add float resistors and calculate temperatures:

<F12 Root Menu> → Model → Amb + Float → Isoltd->Fix → "Room Amb" → Natural → Both Sides → All In Wind → USE

click 

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

You should obtain T_{junct} = 66.72°C, a dramatic reduction. Ground and power planes have an important impact on cooling, *even when there are no thermal vias.*

Isolating a layer in the stackup

In a moment, you will modify the via density for the front laminate layer. Of course, it's very important that you modify the front laminate layer and not one of the other laminate layers . So you will start by isolating the front laminate layer.

Enter these commands:

<F12 Root Menu> → Visibility → Isolate → Layer

You will reach the Layer menu:

```
  LAYER
1 Copp>1
2 Copp>2
3 Copp>3
4 Copp>4
5 Lamin>1
6 Lamin>2
7 Lamin>3
8 Enter Prefix
```

This menu provides the necessary choices for isolating a copper or laminate layer in a four layer board. Since you will be modifying the front laminate layer, the correct choice is "Lamin>1". If you are modeling a board with more than 4 copper layers, you would use "Enter Prefix" to specify the layer. For example, you could isolate a 4th laminate layer with **Enter Prefix → "Lamin>4"**.

Note that if you have two board stackups in your Sauna model, you should use label prefixes to distinguish between the two boards. So you might use a label prefix of "Bd1:" for the first board stackup and a prefix of "Bd2:" for the second stackup. Then the first copper layer in the first stackup would be "Bd1:Copp>1". You could isolate the layer with **Enter Prefix → "Bd1:Copp>1"**. In fact, you could isolate the entire board stackup with **Enter Prefix → "Bd1:"**. *Membership in a Sauna layer is based entirely on the starting characters (prefix) of the assembly label.*

Finish isolating the front laminate layer with:

Lamin>1

With this visibility change, you will see only the front laminate board assembly and the DPAK. All other laminate layers are turned off. All copper pads and traces are also turned off. To verify, switch to a top view in shade mode.

click Top ➔ ***click*** 

The top view shows only the DPAK and the front laminate layer. It is important to note that **Sauna links enhanced sources to the board assemblies, not to the traces and pads**. (If you delete the front laminate layer, the DPAK will be deleted automatically.)

Step #10: change the via density

While you just saw that internal planes without vias can improve thermal performance, it's safe to say that temperatures will be even cooler with vias underneath the heat source.

Note that there is no need to delete float resistors when modifying vias. You must delete the float resistors whenever there is a change to the outer surface of the board stackup. But vias are an internal property of the laminate layers, so nothing changes on the outer surface.

Switch to wireframe mode and return to a front view:

click  ➔ ***click*** Front

Zoom in to match Figure 2-32:

<F3 Zoom In> ➔ *zoom in to match Figure 2-32*

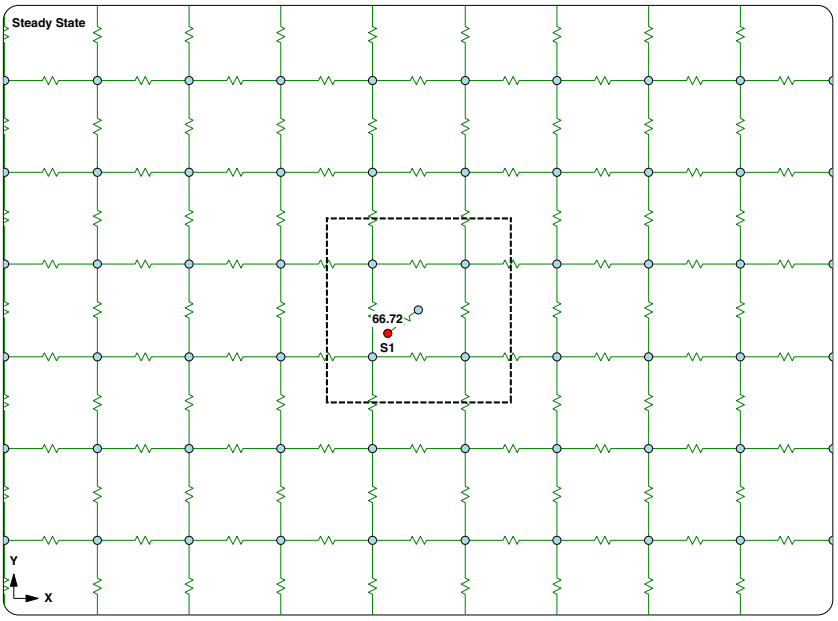


Figure 2-32: Zooming in on the DPAK

Activate the display of via density:

<F6 Setup> ➔ Display ➔ Node ➔ Via Density ➔ Vias/In2

You will see "0i", for 0 vias per inch^2, displayed across the board. Currently there are no vias. (The node at the center of the body assembly does not have a number because the node belongs to the body assembly and cannot have a via density.)

Now you need to visualize the exact nodes to be modified. Activate the outlining of diepads:

<F6 Setup> → Display → Node → Outlines → Enhan Diepad

With this change you will see a red rectangle which indicate the limits of the diepad. For a DPAK, the outline is the same as the overall part, as it is assumed that the copper slug is the same size as the overall package (in reality, the slug is usually a bit smaller, but Sauna ignores this).

Now you can easily change the via density to "High":

<F12 Root Menu> → Edit → Plate/Board → Board Props → Vias → Density → High (100) → Node Group → Select Regn → *grouping rectangle matches red outline of DPAK* → USE

The via density will be changed to "100i" for the selected nodes. Also, Sauna indicates that "via density modified for 4 nodes".

The via density change is complete. Restore visibility and calculate temperatures:

<F6 Setup> → Display → Use Default

click  **→ *click*** 

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

With the vias, you should obtain T_{junct} = 50.25°C, which is roughly 40% cooler than before. Note that the biggest gains came from adding the internal planes, not from adding the vias.

Since the board in Figure 2-27 does not have components on the back side, you have finished with the checklist.

Comparing the planar and detailed stackup models

You have obtained $T_{junct\text{-}planar}$ = 45.91°C and $T_{junct\text{-}stackup}$ = 50.25°C. The detailed stackup temperature is higher, because the planar model uses the optimistic assumption that there is no ΔT between the front and back. But the temperatures are fairly close. $T_{junct\text{-}planar}$ is just 17% cooler than the detailed stackup model.

So what can be concluded? If you are only interested in multilayer boards with DPAK-style components and lots of thermal vias, then the planar model may be all that you need. But most boards are not like this. You will certainly not get good results if you use the planar method to analyze single layer boards. The DPAK has a full size copper slug, but many components have partial copper slugs. And then there are components like PLCC LED's that are cooled primarily through the leads. So the planar method has limitations.

As a general guideline, use the planar method for first-pass analysis. If temperatures are well within your goals, you do not need to perform further analysis. But if there are concerns, you should proceed to the detailed stackup method.

What-if: impact of DPAK traces for multilayer board, saving model

Earlier in the exercise, you deleted the three 25 mm traces and saw an 11% increase in junction temperature. Now you will do the same thing with the planar model.

Working on your own, delete the fixed nodes and float resistors. Then delete the three traces. Recreate float resistors and calculate temperatures.

You should obtain T_{junct} = 50.47°C, which is an increase of just 0.2°C, or 0.9%. So for a DPAK package on a multilayer board with vias, the traces do very little.

Since the traces have such a small impact, they will stay deleted for the rest of exercise.

This model will be used in another exercise. Save the model as "dpak_four_lyr.smf":

<F12 Root Menu> → File → Save As → ***type "dpak_four_lyr" in File name box***
→ ***click Save button***

Adding dual SOIC devices

Up until now, you have been working with a simple model with a single DPAK package power component. Now you will add other types of components. You will start by adding two 16 lead SOIC devices. This type of package is shown in Figure 2-33:

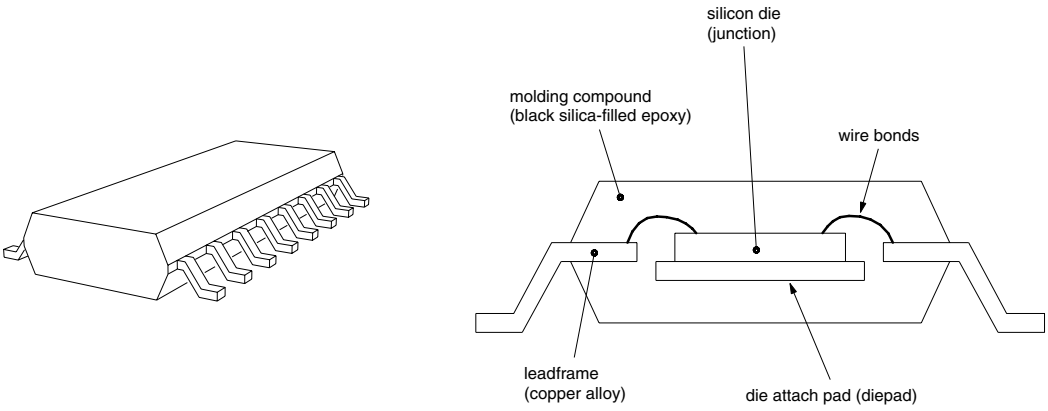


Figure 2-33: 16 pin SOIC package

With a standard SOIC package, the die and diepad are fully internal to the part. So heat flow through the leads and traces is an important part of cooling. While you could do a crude approximation with a basic heat source, an enhanced heat source is really a requirement to correctly model this type of part.

You will add SOIC devices in the configuration shown in Figure 2-34 on the next page:

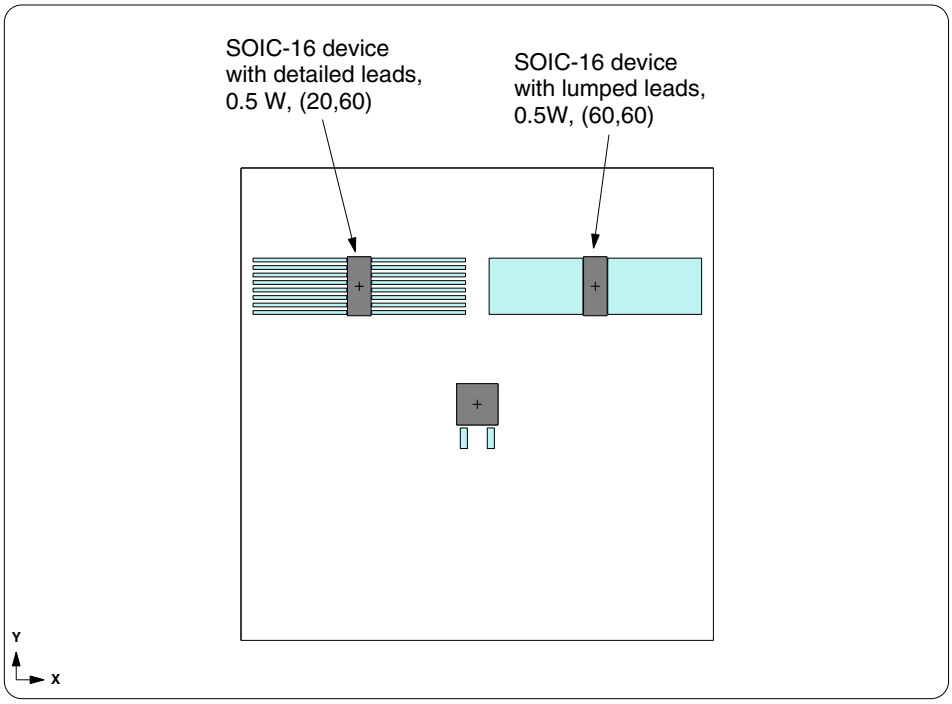


Figure 2-34: SOIC-16 devices with detailed and lumped leads

Note that the left SOIC is modeled with "detailed" leads, which means there is a trace for each component lead, while the right SOIC uses the "lumped" option. The lumped option provides a way to simplify the model. You are modeling 16 lead devices at the moment. But since quad IC's can have 256 or more leads, simplified models are desirable.

Adding traces and pads for SOIC devices

Since you are modifying the outer surface of the stackup, delete the existing ambients and float resistors:

click 

<F12 Root Menu> → Delete → Node → Fixed → All In Wind → USE

As for DPAK's, Sauna makes it easy to create the pads for the SOIC package components. Begin creating pads with:

<F12 Root Menu> → Model → Assembly → Trace/Pad → Trap Trc/Pad
→ *trap any trace or pad on front layer*
→ Pad Library → Single/Dual → SOIC Narrow → 16

You will reach the Pad Type menu:

```
   PAD TYPE
>1 Lumped
 2 Detailed
 3 Detail/Flare
```

This is the menu for choosing between the "detailed" and "lumped" options shown in Figure 2-34. The "detailed" option is straightforward and is used to create 16 individual lead pads and 16 traces. For "lumped", the lead pads and traces are combined together into larger pads. To compensate for the greater copper area, the copper coverage is reduced to approximately 50%.

You will start with the left SOIC, so you will use the detailed option:

Detailed

Now you will reach the Trace Length menu:

```
 TRACE LENGTH
1 Pad Only
2 5 mm/0.2"
3 10 mm/0.4"
4 15 mm/0.6"
5 25 mm/1.0"
6 35 mm/1.4"
7 50 mm/2.0"
8 Enter
```

As discussed earlier in the exercise, from a thermal standpoint, there is almost no benefit to having traces longer than 25 mm. You also saw that 15 mm traces were nearly as effective as 25 mm traces. So you will use 15 mm traces for the SOIC components. Continue with:

15 mm/0.6" → No

You will reach the Rotation menu for choosing between 0 degrees and 90 degrees. You are probably not sure which selection to use. Check the reference picture for this menu:

click Picture

You will see the picture shown in Figure 34-b. Clearly you want 90 degree rotation.

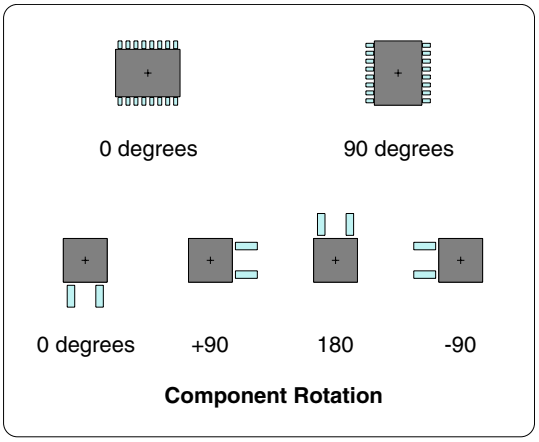


Figure 34b: Reference picture showing component rotation

After clearing the reference picture, complete creation of the pads with:

90 Degrees → Coords/Trap → "20,60"

The traces and pads will be created. To better see the newly created pads and traces, isolate the front copper layer:

<F12 Root Menu> → Visibility → Isolate → Layer → Copp>1

Only traces and pads on the front layer will be visible. Next, zoom in to match Figure 2-35:

<F3 Zoom In> → *zoom in to match Figure 2-35*

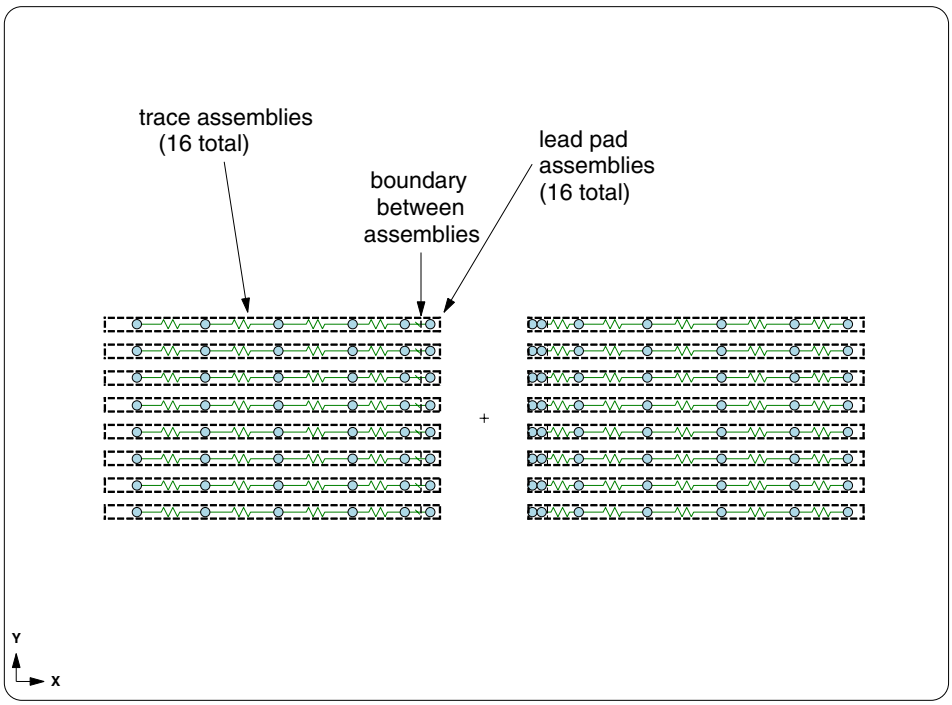


Figure 2-35: Lead pads and traces for SOIC 16 component

Sauna has created a total of 32 assemblies (16 lead pads and 16 traces). However, it probably looks to you like 16 assemblies. That's because Sauna combines joined rectangular assemblies into superassemblies and the constituent assemblies are separated by just a thin dashed line. This approach is discussed in some detail in *Intermediate Exercise 1: Superassemblies And Basic Slicing*. For now, just be aware that a total of 32 assemblies were created.

Restore visibility and zoom out:

click  **→** ***click*** 

Now it's time to try the lumped option. Create pads for the right SOIC-16 device:

<F12 Root Menu> → Model → Assembly → Trace/Pad → Trap Trc/Pad
→ *trap any trace or pad on front layer* → Pad Library → Single/Dual → SOIC Narrow
→ 16 → Lumped → 15 mm/0.6" → No → 90 Degrees → Coords/Trap → "60,60"

The lumped pads and traces will be created. As before, isolate the front copper layer and zoom in:

<F12 Root Menu> → Visibility → Isolate → Layer → Copp>1

<F3 Zoom In> → *zoom in to match Figure 2-36*

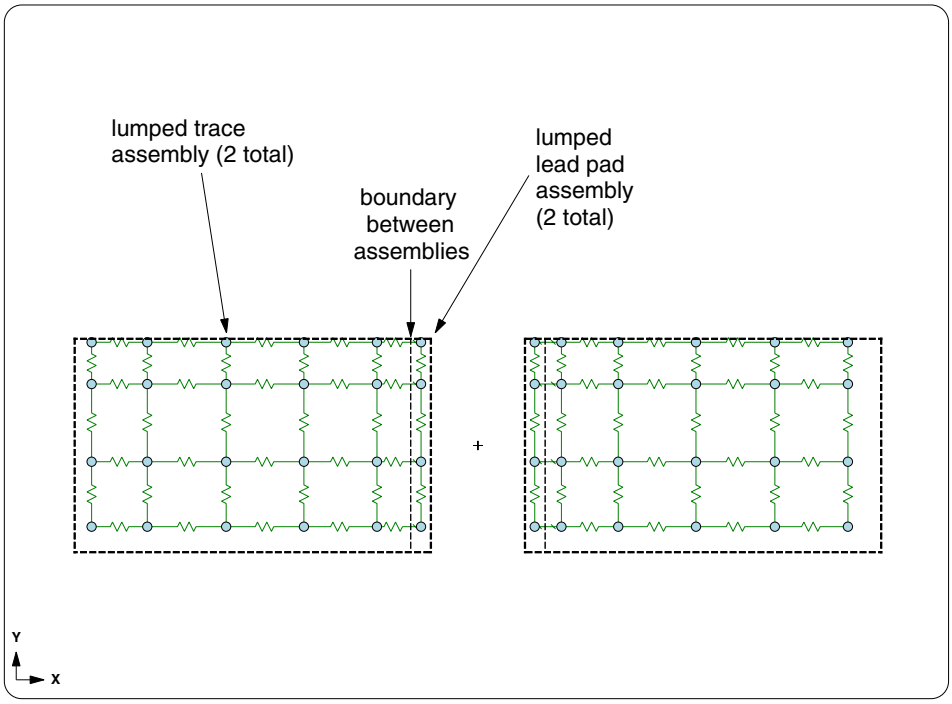


Figure 2-36: Lead pads and traces with lumped option

As you can see from Figure 2-36, Sauna created 4 assemblies (2 lead pad assemblies and 2 trace assemblies). The thin dashed line between assemblies is clearly visible in this picture.

Now activate copper coverage:

<F6 Setup> → Display → Node → Cu Coverage → On

You will see "53", for 53% copper coverage, for all of the nodes. The reduced copper coverage compensates for the larger area of the lumped traces and pads. With 53% copper coverage, the end-to-end resistance of the lumped traces is identical to the end-to-end resistance of the detailed traces.

Turn off copper coverage, restore visibility and zoom out:

Off

click  **→** ***click*** 

In the next section you will add SOIC-16 devices to both sets of pads. Since the SOIC components and pads are exactly symmetric on the board, the junction temperatures should be similar, which would validate the lumped approach.

Adding SOIC-16 devices

Begin adding the first component:

<F12 Root Menu> → Model → Heat Input → Enhanced Src → Single/Dual → ".5" → "S2" → SOIC Narrow → 16 → Middle

You will reach the Diepad Area menu:

```
  DIEPAD AREA
>1 Typical/36%
 2 Typical/25%
 3 Specify
```

With this menu you are specifying the area of the die attach pad (diepad) shown in Figure 2-33. The area of the diepad has a definite effect on heat transfer to the top of the component, as well as downward into the board. Unfortunately, there is a good chance that this parameter is unavailable, as it's almost never found on a datasheet. You may be successful (maybe) if you ask the component manufacturer, or you could cut open the part with a fine bladed saw. But if you don't have this information, just use the typical value (area of diepad is 36% of the component body area).

Continue with:

Typical/36% → Typ (0.1 mm)

Once again, you will reach the R_Lead_Pad menu:

```
  R LEAD PAD
>1 Typ-1500 C/W
 2 Enter Resis
 3 Enter R_para
 4 No Lead Conn
```

Earlier in the exercise, you used "Typ-1500 C/W" with the DPAK. You also saw that heat transfer through the leads was not hugely important because temperatures only increased by 11% when the traces were deleted on a single layer board. However, for components that do not have an external copper pad (heat slug), $R_{junct\text{-}to\text{-}lead\text{-}pad}$ is an important thermal parameter. The recommended approach is to obtain $R_{junct\text{-}to\text{-}lead\text{-}pad}$ by reverse engineering the $R_{junct\text{-}to\text{-}ambient}$ (R_{ja}, θ_{ja}) from the component datasheet. This is covered in detail in *Intermediate Exercise 3: More On Circuit Board Modeling* in the section "Obtaining $R_{junct\text{-}to\text{-}lead\text{-}pad}$ from $R_{junction\text{-}to\text{-}ambient}$" . Sauna has special tools for this task and it should only take a few minutes to obtain $R_{junct\text{-}to\text{-}lead\text{-}pad}$. For now, however, you will simply use the default of "Typ-1500 C/W" which will provide a good first pass result. Continue with:

Typ-1500 C/W → Ref Point → *trap reference point for detailed pads*

The component will be created and Sauna will indicate that "Enhanced heat source created, 16 lead connections".

It's interesting to get an Info report for the enhanced source:

<F7 Info> → Trap → Node → Heat Source → *trap S2 heat source*

On the second page, under "-- Junction To Lead Pad Resistance --", there is information on the number of lead pad connections and the resistance values, with $R_{average\text{-}to\text{-}pad}$ = 1500°C/W and $R_{parallel\text{-}to\text{-}pad}$ = 93.75°C/W. This is important information to check. (Although you have used uniform $R_{junct\text{-}to\text{-}lead}$ in this exercise, *Sauna let's you use a different resistance for every lead pad*, an important feature for modeling components with heatsinking leads.)

Clear the Info report and add the right component:

<F12 Root Menu> → Model → Heat Input → Enhanced Src → Single/Dual → ".5" → "S3" → SOIC Narrow → 16 → Middle → Typical/36% → Typ (0.1 mm) → Typ-1500 C/W → Ref Point → ***trap reference point for lumped pads***

The right heat source will be added with the message "Enhanced heat source created, 2 lead connections". As before, get a report for the newly added heat source:

<F7 Info> → Trap → Node → Heat Source → ***trap S3 heat source***

Once again, look at the section "-- Junction To Lead Pad Resistance --" on the second page. With the lumped pads, $R_{average\text{-}to\text{-}pad}$ is lower (187.50°C / W vs. 1500°C / W), but $R_{parallel\text{-}to\text{-}pad}$ = 93.75°C / W, the same as before.

Completing the model and comparing lumped vs. detailed

Clear the report, then create float resistors and calculate temperatures:

<F12 Root Menu> → Model → Amb + Float → Isoltd->Fix → "Room Amb" → Natural → Both Sides → All In Wind → USE

click 

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

When complete, you should obtain $T_{j\text{-}SOIC\text{-}left}$ = 81.28°C and $T_{j\text{-}SOIC\text{-}right}$ = 78.98°C. The temperatures are within 2.3°C, showing that lumped leads provide similar results.

Aligning the mesh to SOIC devices, is it required?

Earlier in the exercise, you aligned the mesh to the DPAK source. You may have wondered: *is this necessary for the SOIC devices?* The answer is "no". This is only required for heat slug devices (exposed copper pad soldered to board).

Extend or shorten a group of traces

In this section, you will shorten the 16 traces for the S2 SOIC device. The new trace length will be 10 mm, so a reduction of 5 mm.

Earlier in the exercise, you extended the DPAK traces with **Edit → Plate/Board → Dimensions → Trace/Pad → Shift Endpt...** This works fine, but you can only modify one trace at a time. This was not a problem with a DPAK but it gets tedious when you must extend 16 traces.

Instead of the trace-specific "extend" command, you will use commands that work for any assembly. As a first step, delete the float resistors:

click 

<F12 Root Menu> → Delete → Node → Fixed → All In Wind → USE

Instead of shifting an endpoint, you will modify the overall X-dimension of the trace assemblies. Enter these commands (you do not need to zoom in):

<F12 Root Menu> → Edit → Plate/Board → Dimensions → Modify X → Enter Delta → "-5" → End → Select Regn → ***use grouping rectangle similar to Figure 2-37*** **→ USE**

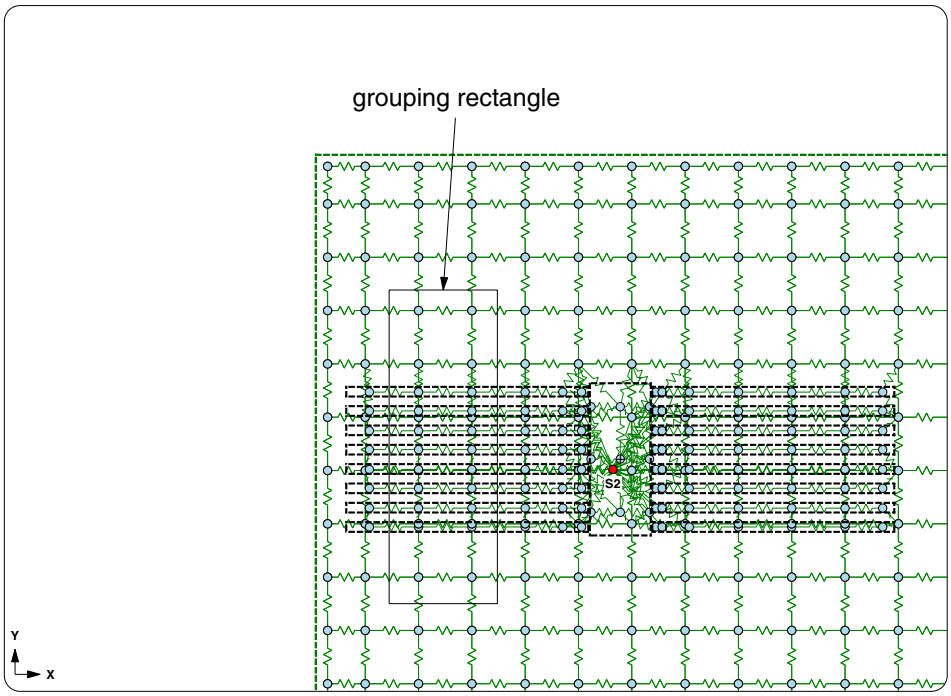


Figure 2-37: Grouping rectangle for left 8 traces

The left traces will be shortened by 5 mm. A couple of comments should be made. First, notice that you used "End" on the Keep Point menu. If you are uncertain as to why you did this, see the reference picture at **<F11 Help> → Ref Picts → Basics → Keep Point**. Second, be sure to only select traces, not the lead pads.

Now modify the right traces, while keeping the origin point:

<F12 Root Menu> → Edit → Plate/Board → Dimensions → Modify X → Enter Delta → "-5" → Origin → ***place right 8 traces in group*** **→ USE**

The right 8 traces should be shortened by 5 mm.

Now add float resistors and calculate temperatures:

<F12 Root Menu> → Model → Amb + Float → Isoltd->Fix → "Room Amb" → Natural → Both Sides → All In Wind → USE

click 

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

You should obtain $T_{S2\text{-junct}}$ = 81.94°C, a modest increase of 0.7°C from the model with 15 mm traces. So, for a multi-layer board at least, you do not need long traces, even for the SOIC.

Adding a quad flatpack with heat slug

Now you will add a quad flatpack to achieve the board layout shown in Figure 2-38:

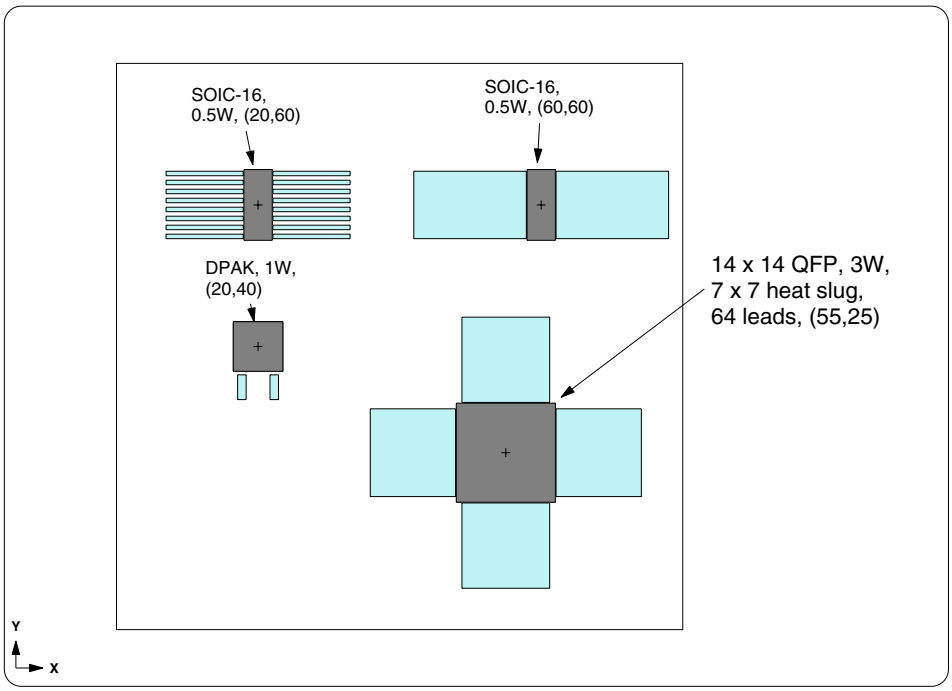


Figure 2-38: Board with quad flatpack

If you look at Figure 2-38, you will see that the DPAK has been moved to the left by 20 mm. So you will move the DPAK source and associated pads in the next section.

Moving an enhanced source

It is definitely more complicated to move an enhanced source than a basic source. Here are the steps:

1. If necessary, delete float resistors and ambient nodes.
2. If necessary, edit the via density underneath the device to be moved.
3. Disconnect the heat source with **Delete → Special Del → Disconn Src...**
4. For the traces and pads, delete the stack joins to the board. This is generally done with **Delete → Join → Stack → Grp To Model...**
5. Move the traces and pads.
6. Move the heat source.
7. Join the pads to the laminate layer with **Model → Join → Stack → Copper Layer**.
8. Reconnect the heat source with **Edit → Heat Input → Reattach**.
9. If necessary, modify via density.

The list is a bit intimidating, but it's pretty easy once you understand the method.

The first step is to delete float resistors:

click 

<F12 Root Menu> → Delete → Node → Fixed → All In Wind → USE

The second step is the removal of vias. Since the DPAK is currently the only component with vias, you can remove vias from the entire front laminate layer:

<F12 Root Menu> → Edit → Plate/Board → Board Props → Vias → Density → None → Entire Board → Group → Select 1 → "Lamin>1" → USE

Now you will "disconnect" the heat source. There has been a disconnect command in Sauna for many years, but most users do not use this feature. The disconnect command deletes all the resistors between the heat source and the underlying pads and laminate. Disconnect the DPAK with:

<F12 Root Menu> → Delete → Special Del → Disconn Src → Select 1 → *trap S1-DPAK source node* → USE

Next, delete the joins between the DPAK pads and the front laminate layer:

<F12 Root Menu> → Delete → Join → Stack → Grp To Model → Trace/Pad → Select Regn → *use grouping rectangle from Figure 2-39* → USE

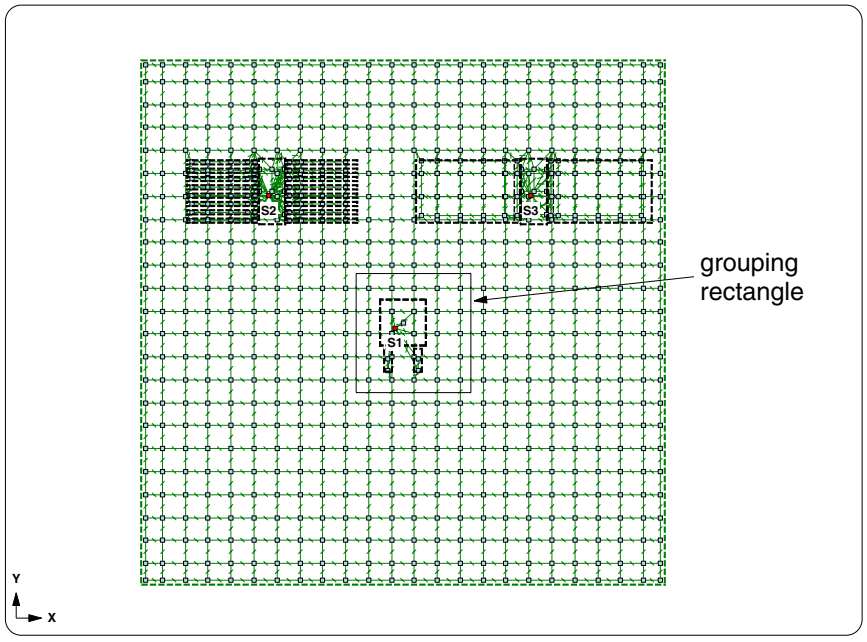


Figure 2-39: Grouping rectangle for deleting DPAK stack joins

Sauna will indicate that "3 joins were deleted".

Move the pads to the left by 20 mm:

<F12 Root Menu> → Move/Copy → Move → Assembly → Plate → Select Regn → *use grouping rectangle from Figure 2-39* → USE → Dx → "-20"

The pads will be moved. Now move the heat source:

<F1 Window> → Refresh

<F12 Root Menu> → Move/Copy → Move → Node → Heat Source → Any Source → Select 1 → *trap S1 source* → USE → Dx → "-20"

When you move an enhanced source node, the body assembly will also be moved. You can see this if you switch into shade mode:

click 

Now you need to recreate stack joins. You can use the command for re-joining an entire copper layer:

<F12 Root Menu> → Model → Join → Stack → Copper Layer → *trap any trace or pad on front layer*

Sauna will indicate "39 possible joins: 36 already joined, 3 new joins". Reconnect the heat source:

<F12 Root Menu> → Edit → Heat Input → Reattach

Resistors will be created between the S1 source and the copper pads.

In the last step of the checklist, you would normally modify the via density. You will make this change later, after adding the QFP.

Now that the DPAK device and pads have been moved, you are ready to add the QFP with heat slug.

Adding the QFP with heat slug

The QFP has a 7 x 7 heat slug in the center, so you will create a matching 7 x 7 pad on the circuit board. Create the pads with:

<F12 Root Menu> → Model → Assembly → Trace/Pad → Trap Trc/Pad → *trap any trace or pad on front layer* → Pad Library → Quad → MQFP → 14 x 14 → 64 Leads → Lumped → 10 mm/0.4" → Yes → "7,7" → Coords/Trap → "55,25"

The pads will be created with a center 7 x 7 pad for the heat slug. With 64 leads, it makes sense to use lumped leads.

Begin creating the enhanced source:

<F12 Root Menu> → Model → Heat Input → Enhanced Src → Quad → "3" → "S4" → MQFP → 14 x 14 → 64 Leads → Heat Slug

You will reach the Diepad Area menu:

```
  DIEPAD AREA
>1 Use Brd Pad
 2 Typical/25%
 3 Typical/36%
 4 Specify
```

This Diepad Area menu is different from earlier in the exercise. When modeling a heat slug component, the diepad will usually have the same dimensions as the solder pad on the board. Continue with:

Use Brd Pad → Typical

You will reach the Gap To Board menu:

```
  GAP TO BOARD
>1 Typ (0.1 mm)
 2 0.02mm/.001"
 3 0.05mm/.002"
 4 0.15mm/.006"
 5 0.20mm/.008"
 6 0.25mm/.010"
 7 0.50mm/.020"
 8 Enter
```

For the resistors to the heat slug pad, Sauna assumes a solder interface. But there is also a portion of the component with an air gap. This menu is used to specify that air gap. Finish with:

Typ (0.1 mm) → Typ-1500 C/W → Ref Point → *trap QFP ref point*

The QFP heat source will be created.

At the moment, the circuit board is aligned to the DPAK's previous position. Since the QFP is dissipating 3W, and is likely a more expensive component, it makes sense to align to this component:

<F12 Root Menu> → Edit → Plate/Board → Remesh/Align → Align Mesh → Heat Source → 4 Node Conn → *trap S4-QFP heat source node* → All In Wind → USE

The circuit board will be aligned to the QFP. Actually, it's fairly easy to align to both the QFP and the DPAK. You just need to do some simple slicing. The method is explained in *Intermediate Exercise 3: More On Circuit Board Modeling* in the "Aligning to multiple heat sources" section.

Add float resistors:

<F12 Root Menu> → Model → Amb + Float → Isoltd->Fix → "Room Amb" → Natural → Both Sides → All In Wind → USE

click 

You still need to add vias, but go ahead and perform a preliminary calculation:

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

You should obtain $T_{S1\text{-}DPAK}$ = 90.21°C and $T_{S4\text{-}QFP}$ = 111.30°C.

Adding vias for the QFP and DPAK devices

In the final part of this exercise, you will add vias underneath the QFP and DPAK. The procedure is the same as before. As mentioned earlier, you do not need to delete float resistors.

Begin by isolating the laminate layer:

<F12 Root Menu> → Visibility → Isolate → Layer → Lamin>1

Next, zoom in to match Figure 2-40:

<F3 Zoom In> -> *zoom in to match Figure 2-40*

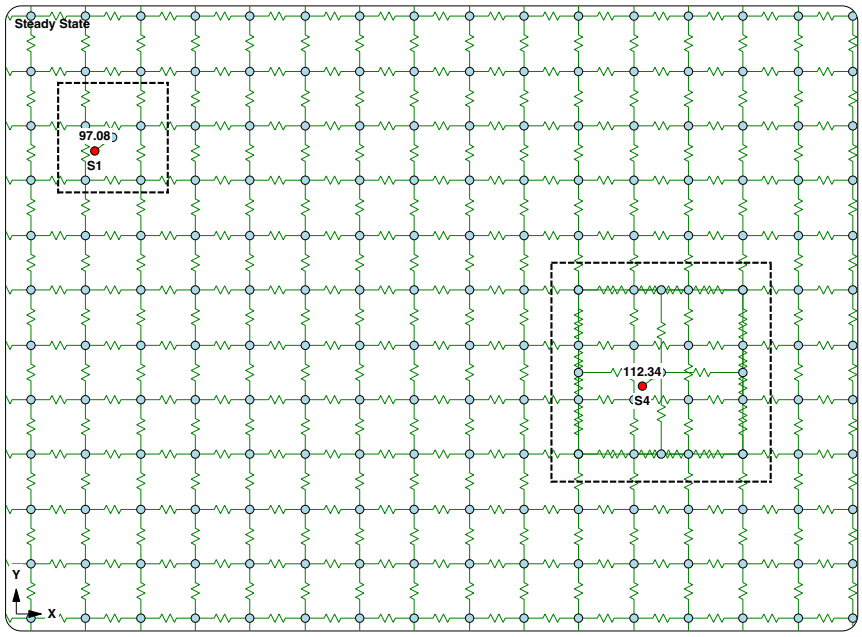


Figure 2-40: Zooming in on DPAK and QFP

As before, activate the display of via density and the outlining of diepads:

<F6 Setup> → Display → Node → Via Density → Vias/In2

<F6 Setup> → Display → Node → Outlines → Enhan Diepad

Now you can easily change the via density to "High" for both the QFP and DPAK:

<F12 Root Menu> → Edit → Plate/Board → Board Props → Vias
→ Density → High (100) → Node Group
→ Select Regn → *grouping rectangle matches red outline of QFP*
→ Select Regn → *grouping rectangle matches red outline of DPAK* → USE

The via density will be changed to "100i" for the selected nodes. Also, Sauna indicates that "via density modified for 8 nodes".

The via density change is complete. Restore the default display setup, turn on all layers and zoom out:

<F6 Setup> → Display → Use Default

click  **→** ***click*** 

Calculate temperatures:

<F12 Root Menu> → Analyze → Calc Temps → Steady → "25"

With the vias, you should obtain $T_{S1\text{-}DPAK}$ = 70.73°C, $T_{S2\text{-}SOIC}$ = 89.74°C, $T_{S3\text{-}SOIC}$ = 88.37°C and $T_{S4\text{-}QFP}$ = 95.67°C and . When the 3W QFP device was added to the board, the total dissipation increased from 2W to 5W. Although the wattage more than doubled, the DPAK and the SOIC's temperatures only increased by 10-15°C. This is often the case for circuit boards, where components tend to be somewhat thermally isolated from each other.

Saving the model

This model will be used in *Intermediate Exercise 3: More On Circuit Board Modeling*. Save the model as "qfp_dpak.smf":

<F12 Root Menu> → File → Save As → ***type "qfp_dpak.smf" in file name box → click Save button***

This exercise is now complete. You should delete the model:

<F12 Root Menu> → Delete → Everything → ***click Yes button***

More details on enhanced sources

This exercise has taught you how to use enhanced heat sources. However, there has been little discussion of modeling assumptions and simplifications. If you are interested in this subject, please see the section "All About Enhanced Heat Sources" in the Using Sauna chapter.

Wrapping up and looking ahead

Congratulations on successfully completing this exercise. This is the longest exercise in the entire manual. You have created a variety of models, starting with a quick planar representation and culminating with a 4 copper layer stackup with individual traces and pads, thermal vias and several different component types. With the tools that Sauna provides, you can create models and perform simulations much more quickly than with other available thermal packages. You can use Sauna to determine the proper spacing between components, specify the required number of thermal vias, manage the area and shape of heatsinking pads, and much more.

Of course there's a reason why the exercise is more than 30 pages long, it's a complicated subject. And there's still more to learn. For this reason, if you expect to do a significant amount of board modeling, it is strongly recommended that you work through *Intermediate Exercise 3: More On Circuit Board Modeling.*

Here are some of the topics presented in *Intermediate Exercise 3: More On Circuit Board Modeling*:

1. Obtaining $R_{junction\text{-}to\text{-}lead\text{-}pad}$ from $R_{junction\text{-}to\text{-}ambient}$. This section teaches you how to obtain the thermal resistance between the device junction and individual lead pads. You start with the $R_{junction\text{-}to\text{-}ambient}$ (R_{ja}, θ_{ja}) value found on most datasheets.

2. Aligning a board stackup to multiple heat sources.

3. Modeling flip chip components.

4. Placing a finned heat sink on top of an enhanced heat source.

5. Modifying the internal planes of a board stackup

6. Creating enhanced heat sources for components which are not found in Sauna's library.

These are important topics. Please take the time to work through *Intermediate Exercise 3: More On Circuit Board Modeling*.

If your company uses metal core (IMS) boards, be sure to see *Intermediate Exercise 11: Surface Assemblies And Metal Core Boards*.